Amendments to the Specification:

Please replace original paragraph [20] with the following paragraph [20]:

[20] FIG. 4 is a functional block diagram of a test system 400 including a test management unit (TMU) 21, which may be formed from a Field Programmable Gate Array (FPGA), and which operates as a test pattern decoder to interface multiple chip pins 23 of a DUT 1 to a single test channel 27 of a tester 20 according to one embodiment of the present invention. Only one test channel 27 of the tester 20 is shown in Fig. 4, although the tester includes a number of such test channels coupled to the TMU 21. A compression-decompression scheme as previously discussed can be implemented on the TMU 21 such that the test channel 27 can input a relatively small number of bits and then the TMU can decompress the small number into a larger number of bits for input to multiple scan chains (not shown in Fig. 4) within the DUT 1. Specifically, m bits of an output-disabled-encoded-I/O signal EN-I/O* are fed to the TMU 21. The TMU 21 decodes the output-disabled-encoded-I/O signal EN-I/O* into n bits of an output-disabled-decoded-I/O signal DE-I/O*. Here, $m<n<2^{**}m+1$. The n bits of the output-disabled-decoded-I/O signal DE-I/O* are then fed into respective scan chains within the DUT 1. In this way, each scan chain has its own unique pattern of input data defined by the corresponding nth bits of the DE I/O* signal.

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Please replace original paragraph [23] with the following paragraph [23]:

[23] In operation, the tester 20 initially applies the OFR-In signals to the DUT 1 to initialize the contents of the OFR 22, and also applies the EN-I/O* signals to the TMU 21 which, in turn, decodes these signals to develop the DE-I/O* signals that are applied the pins 23 of the DUT 1. During testing, the tester 20 applies required test data, address and control signals (not shown) to the DUT 1 to control the device as required, as will be appreciated by those skilled in the art. The tester 20 thereafter receives the OFR-Out signals from the DUT 1 and determines whether these signals indicate the DUT 1 is operating properly. Note that the OFR-Out signals of Fig. 4 are intended to indicate generally output from the DUT 1 to the tester 20 during testing, and are not limited to a signature being output from the OFR 22. For

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example, in functional testing of the DUT **1** the OFR **22** may not be used and in this *not approved* situation the **OFR-Out** signals correspond to test data being supplied from the DUT **1** *9/6/06 psf* to the tester **20** for analysis to determine whether the DUT is operating properly.

Please replace original paragraph [25] with the following paragraph [25]:

[25] Once the scan test is completed, the scan mode terminates and operation in the functional test mode commences. In the functional test mode, the tester **20** and TMU **21** are reconfigured to execute the desired functional test on the DUT **1**. Typically, such reconfiguration would include assigning a different correlation between the pins **23** of the DUT **1** and the test channels **27** of the tester **20**. If the TMU **21** is implemented in an FPGA, then reconfiguration of the TMU can occur relatively easily in response to the configuration signals **29**, allowing for quickly switching between the scan and functional test modes of operation.

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Please replace original paragraph [27] with the following paragraph [27]:

[27] Although the TMU **21** is shown as being external to the DUT **1** in **Fig. 4**, in another embodiment the TMU is formed inside the DUT **1** (as shown in **Fig. 13**) and not external to the DUT. This could be done, for example, where the TMU **21** is formed by an FPGA formed on the DUT **1**. This would allow on-chip, meaning on the DUT **1**, testing of the DUT while also allowing the tester **20** to program the TMU **21** to define the decoding algorithm being executed by the TMU.

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Please replace original paragraph [30] with the following paragraph [30]:

[30] The OFR cell **32** operates in the compaction mode when the **OEN** signal is active and the **CS** signal is active. In the compaction mode, the OFR cell **32** performs a compacting function, such as an exclusive OR (or XOR) operation, on the **OUT-FP** signal or the scan output data signal **SOD**, with the cell latching the result of this XOR operation and providing this result as the **ODO** signal responsive to the **CLK** signal. The logic to choose the **OUT-FP** signal or the scan output data signal

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SOD is shown in **FIG. 7** and is described below. The OFR cell **32** operates in the shift mode if either of the **CS** or **OEN** signals is inactive, and in the shift mode the cell latches the **ODI** signal and outputs this latched signal as the **ODO** signal responsive to the **CLK** signal. Thus, in the shift mode the OFR cell **32** functions as an individual cell in a conventional shift register, storing an output in the form of the **ODI** signal from an adjacent upstream cell and providing that output in the form of the **ODO** signal to the adjacent downstream cell. The **CS** signal may be viewed as placing the OFR cell **32** in either the compaction or shift mode of operation, with the **OEN** signal providing a further level of control of the cell to determine what whether the type of data--input or output--on the test point **31** is compacted.

Entry approved, 9/6/06

Please replace original paragraph [32] with the following paragraph [32]:

[32]   **FIG. 8** is a diagram illustrating a compactor ~~9~~ 39 made up of the OFR cells **32** of **FIG. 7**. The OFR cell logic **34** of **FIG. 7** is applied to a series XOR gates **36** which feed a series of cyclic shift register cells **CSRC** that make up the cyclic shift register **12**.

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Please replace original paragraph [34] with the following paragraph [34]:

[34]   Referring to **FIG. 11**, a circuit for disabling an output of a bi-directional pin (BDP) **23** (*see* **Fig. 4**) of the DUT **1** is disclosed, and may be contained in the DUT according to one embodiment of the present invention. One problem when testing DUTs **1** with an excessive number of pins **23** is management of bi-directional I/O pins. Direction of operation of bi-directional I/O pins **23** is determined by a state of operation of the functional circuitry in the DUT **1**, and is dynamic in nature. A BDP **23** is coupled to a data input buffer **50** and a data output buffer **45**. The data input buffer **50** is controlled by an input-enable signal **IEN**, and operates to output a functional input signal **IN-FP** responsive to an input signal on the BDP **23** when the **IEN** signal is active, and goes into a high impedance state when the **IEN** signal is inactive. The data output buffer **45** is controlled by an output signal from a NOR-gate **49** fed by an output disable signal **OD** and the output-enable signal **OEN**.

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When either the **OD** signal is active high or the **OEN** signal is inactive low, the NOR gate **49** drives its output inactive low to thereby disable the data output buffer **45** which, in turn, goes into a high impedance state. If the **OD** signal is inactive low and the **OEN** signal is active high, the NOR gate **49** applies a high output to enable the data output buffer **45** which, in turn, provides a functional output signal **OUT-FO-FP** on the BDP **23**. In this way, the output disable signal **OD** may be activated to eliminate output from the BDP pin **23** in the form of the **OUT-FP** signal for the current clock cycle. The associated observability cell **32**, which was previously discussed with reference to **Fig. 6**, also receives the functional output signal **OUT-FO-FP** and operates as previously described responsive to the **OEN** and **CS** signals.

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